SAR Teleconference 1/19/216

We have a grad student to help Olivier with VHDL. Scott and Jordan working on RF and electronics test plan.

Delay line order is underway, will be ordered this evening, Jan 19th. Get receipt to Julian for reimbursement.

Make sure the component box is shielded, won’t affect the issue of the proximity of the box to the structure. Can be done with certain type of shielding tape. Using good shielding for RF in the box will get good marks and look good for the team. Ideal situation would be ports, like a PC where the only inputs to the system is where you plug it in. Or use conduction gaskets.

Some testing on the FPGA has been completed. Progress on the display monitor is being made.

SPDT switch has not gone back for repair yet, will be tested on Friday. Apparently, has already been confirmed to be dead, must be repaired. It does not switch. Hook up the spec any, hook up signal source and move up from 0 to 5 to actually test.

VHDC has come in the mail last night. Will be tested soon, looks like it will definitely fit the FPGA port.